CLAIMS

What is claimed is:

1. A data transmission system, comprising:

a hub including a plurality of adapters;

a crossbar switch coupling said plurality of adapters;

said plurality of adapters including at least a requesting adapter and at least a destination adapter, wherein each of said plurality of adapters includes:

a serial communication controller, further includes:

means for converting a first data frame into serial data before transmitting said serial data to said crossbar switch;

means for converting said serial data received from said crossbar switch into said first data frame before transmitting said first data frame; and

a plurality of data processing systems, including at least a requesting data processing system and at least a destination data processing system, coupled to said hub via said requesting adapter and said destination adapter.

2. The data transmission system according to Claim 1, wherein said adapter further includes:

a control logic for generating a request signal (REQ) to said crossbar switch when said requesting adapter requests transfer of at least said first data frame to said destination adapter.

3. The data transmission system according to Claim 2, wherein each of said plurality of adapters further includes:

a clock multiplier for multiplying a data clock of the system by sixteen and for providing said control logic with timing pulses utilized to transmit said request signal (REQ), wherein said request signal (REQ) is an encoded signal of thirty-two bits.

4. The data transmission system according to Claim 3, wherein said request signal (REQ) includes a first pair of data bytes including sixteen bits defining a destination address of said data frame to be transmitted and a second pair of data bytes including sixteen bits representing a connection time defined by a number of slots to be transmitted.

5. The data transmission system according to Claim 4, wherein said first data byte defining said destination address includes a first bit for each of said plurality of adapters and a second bit set when said destination address corresponds to said destination adapter of said plurality of adapters, said second bit designating a point-to-point connection, a multicast connection, or a broadcast connection.

6. The data transmission system according to Claim 2, wherein said serial communication controller further includes:

means for generating a second data frame, in response to receiving said first data frame, said requesting data processing system coupled to said requesting adapter before transmitting said second data frame to said crossbar switch.

7. The data transmission system according to Claim 6, wherein said generating means in said serial communication controller further includes:

means for generating a second data frame flag to start said second data frame;

means for serializing a plurality of incoming parallel data bytes;

means for computing a frame check sequence (FCS) after serializing said plurality of incoming parallel data bytes; and

means for generating another said second data frame flag to end said second data frame.

8. The data transmission system according to Claim 2, wherein said serial communication controller further includes:

means for converting said second data frame received from said crossbar switch into said first data frame to be transmitted to said destination adapter.

9. The data transmission system according to Claim 8, wherein said converting means further includes:

means for detecting a starting second data frame in an incoming second data frame;

means for checking data integrity of said second data frame by computing a frame check sequence (FCS); and

means for deserializing a plurality of data bits of said second data frame to provide a plurality of data bytes in said first data frame.

10. The data transmission system according to Claim 9, wherein each of said plurality of adapters further includes:

a memory divided into at least two independent areas, a first data processing system-to-switch area organized in a first plurality of buffers for storing at least said first data frame received from a data processing system coupled to said adapter to be transmitted to another data processing system, and a second switch-to-data processing system area organized in a second plurality of buffers for storing said first data frame received from another data processing system.

11. The data transmission system according to Claim 1, wherein each of said plurality of adapters further includes:

a controller for converting said first data frame received in serial form from said requesting data processing system coupled to said coupled adapter into parallel data bytes.

12. The data transmission system according to Claim 11, wherein said controller further includes:

a clock circuit to synchronize operation of said controller;

means for synchronizing said clock circuit during a set of preamble bytes when receiving said first data frame;

means for detecting said first data frame incoming through a delimiter byte of said first data frame;

means for checking data integrity of said first data frame by computing a set of frame check sequence (FCS) bytes;

means for removing a set of protocol information of said first data frame; and

means for deserializing a set of remaining incoming bits of said data frame to provide a set of parallel data bytes.

13. The data transmission system according to Claim 11, wherein said controller further includes:

means for serializing a set of incoming data bytes received from said serial communication controller;

means for generating the protocol information bytes to be included in said first data frame; and

means for computing a frame check sequence (FCS) of said first data frame before transmitting said first data frame to said destination data processing system coupled to said destination adapter.

14. The data transmission system according to Claim 11, further comprising:

an arbiter for taking care of the contention between requests to send from said controller and requests to send from said serial communication controller.

15. The data transmission system according to Claim 1, wherein said crossbar switch further includes:

a scheduler for determining whether or not a request to transmit said first data frame from a data processing system to another data processing system should be granted.

16. The data transmission system according to Claim 15, wherein said scheduler further includes:

an algorithm unit for determining the best data connection to establish at each time based upon the selection of the request amongst all requests received from said plurality of adapters which meets a predetermined criteria.

17. A data transmission system, comprising:

a hub including a plurality of local area network (LAN) adapters;

an asynchronous transfer mode (ATM) crossbar switch coupling said plurality of LAN adapters;

said plurality of LAN adapters including at least a requesting LAN adapter and at least a destination LAN adapter, wherein each of said LAN adapters including:

a serial communication controller, further includes:

means for converting a LAN data frame into serial data implemented as concatenated slots of an ATM cell size in high-level data link control (HDLC) format before transmitting said serial data to said ATM crossbar switch;

means for converting said serial data implemented as concatenated ATM cells received from said ATM crossbar switch into said LAN data frame before transmitting said LAN data frame; and

a plurality of local area networks (LANs), including at least a requesting LAN and at least a destination LAN, coupled to said hub via said requesting LAN adapter and said destination LAN adapter.

18. The data transmission system according to Claim 17, wherein said LAN adapter further includes:

a control logic for generating a request signal (REQ) to said ATM crossbar switch when said requesting LAN adapter requests transfer of at least a LAN data frame to said destination LAN adapter.

19. The data transmission system according to Claim 18, wherein said LAN adapter further includes:

a clock multiplier for multiplying a data clock of the system by sixteen and for providing said control logic with timing pulses utilized to transmit said request signal (REQ), wherein said request signal (REQ) is an encoded signal of thirty-two bits.

20. The data transmission system according to Claim 19, wherein said request signal (REQ) includes a first pair of data bytes including sixteen bits defining a destination address of said LAN data frame to be transmitted and a second pair of data bytes including sixteen bits representing a connection time defined by a number of slots to be transmitted.

21. The data transmission system according to Claim 20, wherein said first data byte defining said destination address includes a first bit for each of said plurality of LAN adapters and a second bit set when said destination address corresponds to an associated LAN adapter of said plurality of LAN adapters, said second bit designating a point-to-point connection, a multicast connection, or a broadcast connection.

22. The data transmission system according to Claim 18, wherein said serial communication controller further includes:

means for generating a high-level data link control (HDLC) frame, in response to receiving said LAN data frame said requesting LAN coupled to said

requesting LAN adapter before transmitting said HDLC frame to said ATM crossbar switch.

23. The data transmission system according to Claim 22, wherein said generating means in said serial communication controller further includes:

means for generating a high-level data link control (HDLC) flag to start said HDLC frame;

means for serializing a plurality of incoming parallel data bytes;

means for computing a frame check sequence (FCS) after said plurality of incoming parallel data bytes; and

means for generating another said HDLC flag to end said HDLC frame.

24. The data transmission system according to Claim 18, wherein said serial communication controller further includes:

means for converting a high-level data link control (HDLC) frame received from said ATM crossbar switch into said LAN data frame to be transmitted to said destination LAN adapter.

25. The data transmission system according to Claim 24, wherein said converting means further includes:

means for detecting a starting high-level data link control (HDLC) frame in an incoming HDLC frame;

means for checking the data integrity of said HDLC frame by computing a frame check sequence (FCS); and

means for deserializing a plurality of data bits of said HDLC frame to provide a plurality of data bytes in said LAN data frame.

26. The data transmission system according to Claim 25, wherein each of said plurality of LAN adapters further includes:

a memory divided into at least two independent areas, a first LAN-to-switch area organized in a first plurality of buffers for storing said LAN data frame received from a LAN coupled to said LAN adapter to be transmitted to another LAN, and a second switch-to-LAN area organized in a second plurality of buffers for storing said LAN data frame received from another LAN.

27. The data transmission system according to Claims 17, wherein each of said plurality of LAN adapters further includes:

a LAN controller for converting said LAN data frame received in serial form from said requesting LAN coupled to said coupled LAN adapter into parallel data bytes.

28. The data transmission system according to Claim 27, wherein said LAN controller further includes:

a clock circuit for synchronize operation of said LAN controller;

means for synchronizing said clock circuit during a set of preamble bytes when receiving said LAN data frame;

means for detecting said LAN data from incoming through a delimiter byte of said frame;

means for checking data integrity of said LAN data frame by computing a set of frame check sequence (FCS) bytes;

means for removing a set of protocol information of said LAN data frame; and

means for deserializing a set of remaining incoming bits of said LAN data frames to provide a set of parallel data bytes.

29. The data transmission system according to Claim 27, wherein said LAN controller further includes:

means for serializing a set of incoming data bytes received from said serial communication controller;

means for generating the protocol information bytes to be included in said LAN data frame; and

means for computing a frame check sequence (FCS) of said LAN data frame before transmitting said LAN data frame to said destination LAN coupled to said destination LAN adapter.

30. The data transmission system according to Claim 27, further comprising:

an arbiter for taking care of the contention between requests to send from said LAN controller and requests to send from said serial communication controller.

31. The data transmission system according to Claim 17, wherein said ATM crossbar switch further includes:

a scheduler for determining whether or not a request to transmit a LAN data frame from a LAN to another LAN should be granted.

32. The data transmission system according to Claim 32, wherein said scheduler further includes:

an algorithm unit for determining the best data connection to establish at each time based upon the selection of the request amongst all requests received from the LAN adapters which meets predetermined criteria.